REMARKS

Claims 1-13 are pending in this application. By this Amendment, claim 1 has merely been amended to more particularly point out and distinctly claim the invention. No new matter is presented. The amendments to claim 1 do not narrow the scope of any element of any claim and are merely cosmetic in nature. Accordingly, claims 1-13 are presented for consideration.

Applicant acknowledges and thanks the Examiner for indicating that claims 7-9 and 12-13 are allowed, and that claims 2-6, 10 and 11 would be allowable over the prior art if amended to overcome the rejection under 35 U.S.C. § 112, second paragraph and to be in independent form. However, Applicant respectfully submits that all of the presently pending claims recite allowable subject matter and therefore, placing claims 2-6, 10 and 11 into independent form is not necessary.

Claims 1-6, 10 and 11 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. By this Amendment, claim 1 has been amended to more particularly point out and distinctly claim the invention. Therefore, the rejection is requested to be withdrawn.

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Sawada (U.S. Patent No. 5,365,481). The Office Action asserted that Sawada discloses all the elements of the claimed invention. However, the Applicant respectfully submits that claim 1 recites subject matter that is neither disclosed nor suggested in Sawada.

Applicant's amended claim 1 recites a semiconductor integrated circuit including a power-on resetting circuit for activating a reset signal in response to an initial supply of a power supply to initialize an internal circuit. The power-on resetting circuit also

inactivates the reset signal after a predetermined period following the initial supply to terminate an initialization of the internal circuit. A timing changing circuit is provided for adjusting the predetermined period in accordance with an internal signal generated in an interior of said timing changing circuit.

The Office Action took the position that Sawada discloses the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest such structure and, therefore, fails to provide the advantages that are provided by the present invention. For example, the timing changing circuit of the present invention adjusts the predetermined period, after which, the reset signal is inactivated in accordance with an internal signal generated in the interior.

As a result of this claimed configuration, the present invention prevents the reset signal from inactivating before the initialization of the internal circuit terminates and allows reliable initialization of the internal circuit. Additionally, the present invention enables adjustment of the time that the reset signal is inactivated without directly measuring the timing of the reset signal by utilizing the voltage generator transistor.

Sawada discloses a DRAM including a power-on reset circuit 17. Power-on reset circuit 17 receives power supply voltage V_{cc} and generates a first power-on reset signal POR1 which goes "H" during a predetermined period. A power-on reset circuit 18 generates a second power-on reset signal POR2 which goes "H" during a variable period. Power-on reset circuit 19 receives POR1 and POR2 and generates a power-on reset signal for forcibly maintaining predetermined circuit units in the DRAM reset state.

In the present invention, a timing changing circuit is provided for adjusting the timing that the reset signal inactivates (in other words, adjusts the predetermined

period) in accordance with an internal signal generated in the interior of the timing changing circuit. However, Sawada only discloses a reset signal which changes the timing it inactivates in accordance to the external signal /RAS, which is an access signal. The external signal /RAS is a signal which the users supply to the semiconductor integrated circuit. This means that Sawada cannot achieve the effect that the present invention has, which is that the inactivation timing, which has deviated due to fluctuations in the manufacturing conditions of the semiconductor integrated circuit, can be adjusted to a normal value. This result is a benefit of the claimed invention.

Thus, in Sawada, there is no disclosure or suggestion of a power-on resetting circuit, which activates a reset signal in response to an initial supply of a power supply to initialize an internal circuit, and inactivates the reset signal after a predetermined period following the initial supply to terminate an initialization of the internal circuit, as recited in claim 1. There is also no disclosure of suggestion of a timing changing circuit that adjusts the predetermined period in accordance with an internal signal generated in an interior of the timing changing circuit, as further recited in claim 1.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claim 1, is not anticipated within the meaning of 35 U.S.C. § 102.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claim 1 (claims 7-9, 12 and 13 already being allowed and claims 2-6, 10 and 11 being indicated as reciting allowable subject matter), and the prompt issuance of a Notice of Allowability are respectfully solicited.

If the application is not in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108397-00042**.

Respectfully submitted,
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Enclosure: Marked-up Version of Amended Claim

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MARKED-UP VERSION OF AMENDED CLAIM

Please amend claim 1 as follows:

1. (Four Times Amended) A semiconductor integrated circuit comprising:

a power-on resetting circuit for activating a reset signal in response to an initial supply of a power supply to initialize an internal circuit, and for inactivating the reset signal after a predetermined period following the initial supply to terminate an initialization of the internal circuit; and

a timing changing circuit for adjusting the predetermined period in accordance with an internal signal generated in [the] an interior of said timing changing circuit.

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